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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,788	03/12/2004	Min-Chul Sun	SAM-0542	8331

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EXAMINER	
WILSON, CHRISTIAN D	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/799,788	SUN ET AL.	
	Examiner	Art Unit	
	Christian Wilson	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 12 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 03122004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: search history.

DETAILED ACTION

Claim Objections

1. Claims 13 and 22 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claims or amend the claims to place the claims in proper dependent form. Claims 13 and 22 recite the limitation "the nickel alloy silicide" which is one part of the Markush group in claims 12 and 21. The limitations listed in claims 13 and 22 do not further limit all possible choices in the Markush group of claims 12 and 21, and therefore they do not further limit the previous claim.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Hoffmann *et al.*

Hoffmann *et al.* (US 2004/0253776) discloses a method of fabricating a semiconductor device comprising forming a MOS transistor **103** at a predetermined region **105** of a semiconductor substrate **102** with a source/drain region **203** and gate electrode **130** over a

channel region **494**, forming a stress layer **213** on the transistor, and annealing the stress layer to increase the tensile stress of the stress layer [0053].

Regarding claim 2, Hoffmann *et al.* further discloses an NMOS device [0016].

Regarding claim 3, Hoffmann *et al.* further discloses forming a nickel silicide on the gate electrode using a salicide technique [0050, 0063].

Regarding claim 4, Hoffmann *et al.* further discloses an insulating stress layer [0056].

Regarding claim 5, Hoffman *et al.* further discloses a silicon nitride layer [0056].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6 – 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffmann *et al.* in view of Brown *et al.*

Hoffmann *et al.* teaches the limitations of claim 1 and 5 as described above including forming a CVD nitride layer, but does not discuss the particular process parameters for the CVD method or annealing method. Brown *et al.* (US 5,264,724) teaches a PECVD deposition method for silicon nitride [column 4, line 37] at a temperature below 500 °C [column 5, line 6] to a thickness of 1000 Å [column 12, line 27], and an annealing process between 400-500 °C [column 5, lines 25-30] in an ambient nitrogen gas. It would have been obvious to one of ordinary skill in the art to use the process steps of Brown *et al.* in the method of Hoffmann *et al.*

since Brown *et al.* teaches that the resulting silicon nitride film is stabilized and has a higher dielectric constant and is impervious to water vapor and ion diffusion [column 3, lines 1-5].

6. Claims 10 – 14 and 19 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffmann *et al.* in view of Ito.

Regarding claims 10 and 11, Hoffmann *et al.* teaches a method of fabricating a semiconductor device comprising forming an isolation layer **120** at a predetermined region of a substrate, forming a MOS transistor **103** at a predetermined region **105** of a semiconductor substrate **102** with a source/drain region **203** and gate electrode **130** over a channel region **494**, forming a nickel silicide on the gate electrode using a salicide technique [0050, 0063], forming a stress layer **213** on the transistor, and annealing the stress layer to increase the tensile stress of the stress layer [0053]. Hoffmann *et al.* discusses forming source/drain regions by doping with an N-type impurity [0017] but does not discuss forming sidewall spacers on the gate electrode or doping an LDD region using the isolation layer as a spacer. Ito (US 6,656,853) teaches forming sidewall spacers and forming an LDD region using the isolation layer as a spacer [Figure 1A]. It would have been obvious to one of ordinary skill in the art to use the doping method of Ito in the method of Hoffmann *et al.* since using sidewall spacers and forming LDD doping are well known methods for shortening the channel length to improve device performance [column 2, lines 60-65].

Regarding claim 12, Hoffmann *et al.* further teaches a pure nickel silicide [0050].

Regarding claim 13, Hoffmann *et al.* further teaches a nickel silicide alloy with Co or Ti [0050].

Regarding claim 14, Hoffman *et al.* further teaches a silicon nitride layer [0056].

Regarding claims 19 and 20, Hoffmann *et al.* teaches a method of fabricating a semiconductor device comprising forming an isolation layer **120** at a predetermined region of a substrate, forming a MOS transistor **103** at a predetermined region **105** of a semiconductor substrate **102** with a source/drain region **203** and gate electrode **130** over a channel region **494**, forming a nickel silicide on the gate electrode using a salicide technique [0050, 0063], forming a stress layer **213** on the transistor, and annealing the stress layer to increase the tensile stress of the stress layer [0053]. Hoffmann *et al.* discusses forming source/drain regions by doping with an N-type impurity [0017] but does not discuss forming sidewall spacers on the gate electrode or doping an LDD region using the isolation layer as a spacer. Hoffmann *et al.* also does not discuss forming an interlayer insulating layer and exposing the stress layer under it. Ito teaches forming sidewall spacers and forming an LDD region using the isolation layer as a spacer [Figure 1A]. Ito also teaches forming an interlayer insulating layer and exposing the stress layer under it [Figures 2A-2C]. It would have been obvious to one of ordinary skill in the art to use the doping method and contact forming method of Ito in the method of Hoffmann *et al.* since using sidewall spacers and forming LDD doping are well known methods for shortening the channel length to improve device performance [column 2, lines 60-65], the contact forming method provides a flat surface while using the silicon nitride stress layer as an etch stop layer [column 4, lines 20-40].

Regarding claim 21, Hoffmann *et al.* further teaches a pure nickel silicide [0050].

Regarding claim 22, Hoffmann *et al.* further teaches a nickel silicide alloy with Co or Ti [0050].

Regarding claim 23, Hoffman *et al.* further teaches a silicon nitride layer [0056].

7. Claims 15 – 18 and 24 – 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoffmann *et al.* and Ito as applied to claims 10 and 19 above, and further in view of Brown *et al.*

Hoffmann *et al.* as modified by Ito teaches the limitations of claims 10 and 19 as described above including forming a CVD nitride layer, but does not discuss the particular process parameters for the CVD method or annealing method. Brown *et al.* teaches a PECVD deposition method for silicon nitride [column 4, line 37] at a temperature below 500 °C [column 5, line 6] to a thickness of 1000 Å [column 12, line 27], and an annealing process between 400-500 °C [column 5, lines 25-30] in an ambient nitrogen gas. It would have been obvious to one of ordinary skill in the art to use the process steps of Brown *et al.* in the method of Hoffmann *et al.* since Brown *et al.* teaches that the resulting silicon nitride film is stabilized and has a higher dielectric constant and is impervious to water vapor and ion diffusion [column 3, lines 1-5].

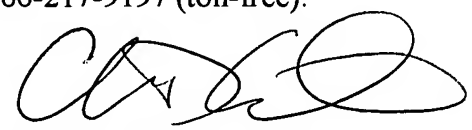
Conclusion

8. A copy of the search history is enclosed.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian Wilson whose telephone number is (571) 272-1886. The examiner can normally be reached on weekdays, 7:30 AM to 4 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Christian Wilson, Ph.D.
Primary Examiner
Art Unit 2891

CDW